Claim 1 claims a method of producing a semiconductor device comprising dry etching an upper layer pattern formed on an insulating film such that at least a part of the insulating film is exposed. After the dry etching, a surface of the insulating film is exposed to a same film formation atmosphere as used to form the insulating film prior to forming additional layers upon the insulating film. Referring to Applicant's Figure 1B as an illustrative example, the upper layer pattern 105 is dry etched to expose at least a part of insulating film 104. Then, a surface of the insulating film 104 is exposed to a same atmosphere as used to form the insulating film 104. This is done prior to forming additional layers upon the insulating film 104.

Accordingly, as described in the specification, by exposing the surface of the insulating film to a same atmosphere as used to form the insulating film, damage that occurred to the surface of the insulating film resulting from the dry etching is removed. (Page 7, lines 11-22).

This is clearly unlike *Miyasaka*, which fails to disclose exposing a surface of an insulating layer to a same atmosphere as used to form the insulating layer after a performing dry etching. Referring to *Miyasaka* Figures 18A-18D, *Miyasaka* discloses forming a silicon oxide insulating layer 13 on an amorphous silicon layer 12 and a substrate 11. As shown in Figure 18A, a mask 22 is formed on the insulating layer 13. And then the insulating layer 13 is patterned using photolithography, as shown in Figure 18B. Next, as shown in FIG. 18C, the surface of the insulating layer 14 is dry etched (Col. 32, lines 27-29) and hydrogenated through hydrogen plasma irradiation (Col. 32, lines 46-49). Then, a silicon nitride insulating layer 14 is formed on the silicon oxide insulating layer 13, as shown in FIG. 18D.

Therefore, unlike Applicant's claim 1, nowhere does *Miyasaka* disclose or even suggest exposing its insulating layer 13 to a same atmosphere as used to form the insulating layer 13 after dry etching. Instead, *Miyasaka* performs dry etching (FIG. 18C) and then hydrogenates the surface of the silicon oxide insulating layer 13 through plasma irradiation (FIG. 18C), and then forms a silicon nitride insulating layer 14 on the silicon oxide insulation layer 13. Unlike Applicant's claim 1, *Miyasaka* does not expose its insulating layer 13 to a same atmosphere as used to form the insulating layer 13 after its dry etching step. Instead, *Miyasaka* merely exposes its insulating layer 13 to hydrogenation and then forms a layer of a different material 14 on top of the insulating layer 13.

Thus, *Miyasaka* fails to disclose or even suggest Applicant's claim 1.

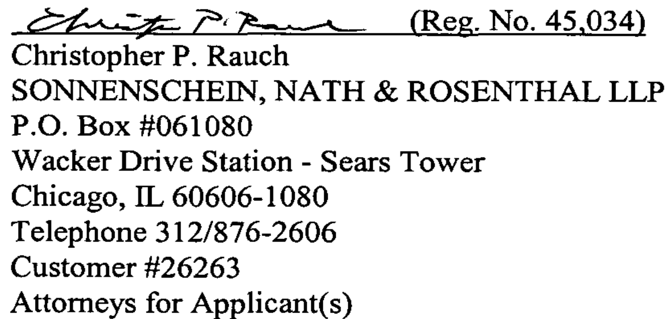
Claim 2 depends directly or indirectly from claim 1 and is therefore allowable for at least the same reasons that claim 1 is allowable.

Applicant respectfully submits the rejection has been overcome and requests that it be withdrawn.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-2 are patentable. It is therefore submitted that the application is in condition for allowance. Notice to that effect is respectfully requested.

Respectfully submitted,



(Reg. No. 45,034)

Christopher P. Rauch
SONNENSCHEIN, NATH & ROSENTHAL LLP
P.O. Box #061080
Wacker Drive Station - Sears Tower
Chicago, IL 60606-1080
Telephone 312/876-2606
Customer #26263
Attorneys for Applicant(s)

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Please amend claim 1 as follows:

1. (Three Times Amended) A method of producing a semiconductor device, the method comprising the steps of:

dry etching an upper layer pattern formed on an insulating film such that at least a part of the insulating film, which is formed above an element separation and a substrate, is exposed; and

after the dry etching, exposing a surface of the insulating film to a same film formation atmosphere as used to form [of] the insulating film prior to forming additional layers upon the insulating film.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited as First Class Mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on July 31, 2003.

(Reg. No. 45,034)
Christopher P. Rauch